WHAT IS CLAIMED IS

1. A nonvolatile semiconductor memory device, comprising:

a memory cell transistor which is configured to store two bits inclusive of a first bit and a second bit at respective ends of an electric charge capturing film;

a comparator which checks a data status by reading data of the first bit; and

a potential switching circuit which changes potential conditions for writing of the second bit in response to whether the data status is 0 or 1.

2. The nonvolatile semiconductor memory device as claimed in claim 1, wherein said potential switching circuit changes a write potential for the second bit in response to whether the data status is 0 or 1.

3. The nonvolatile semiconductor memory device as claimed in claim 1, wherein said potential switching circuit changes a write-verify potential for the second bit in response to whether the data status is 0 or 1.

4. The nonvolatile semiconductor memory device as claimed in claim 1, further comprising a reference cell whose threshold changes in response to whether the data status is 0 or 1.

5. A nonvolatile semiconductor memory device, comprising:

a memory cell transistor which is configured to store two bits at respective ends of an electric charge capturing film; and

a potential switching circuit which supplies a first drain potential to said memory cell transistor at a time of a read operation, and supplies a second drain potential higher than the first drain potential at a time of a write-verify operation.

6. The nonvolatile semiconductor memory device as claimed in claim 5, wherein the second drain potential, when one of the two bits is subjected to the write verify operation, is as high as to be substantially free from influence of another one of the two bits, and is as low as to avoid erroneous writing in said another one of the two bit.

7. A method of writing in respect of a nonvolatile semiconductor memory device, comprising the steps of:

checking a data status by reading data of a first bit from a memory cell transistor which is configured to store two bits inclusive of the first bit and a second bit at respective ends of an electric charge capturing film;

determining potential conditions for writing of the second bit in response to whether the data status is 0 or 1; and

performing a write operation with respect to the second bit by the determined potential conditions.

8. The method of writing in respect of a nonvolatile semiconductor memory device, comprising a step of reading data from a memory cell transistor at a time of a write-verify operation by applying a second drain potential higher than a first drain potential that is applied to the memory cell transistor at a time of a read operation, said memory cell transistor being configured to store two bits at respective ends of an electric charge capturing film.